IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
(3Com Docket No. 06-540)

In re Application of:	)	
	)	
Nathan Henderson et al.	)	
	)	Examiner: Cao, Chun
Serial No.: 09/942,789	)	
	)	Group Art Unit: 2115
Filed: August 29, 2001	)	
	)	Confirmation No.: 2943
For: High Speed Network Interface With Automatic Power Management with Auto-Negotiation	)	

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

DECLARATION PURSUANT TO 37 C.F.R. § 1.131

Dear Sir:

We, Chi-Lie Wang, residing at 941 Westridge Drive, Milpitas, California 95035; and Nathaniel Henderson, residing at 1329 Prevost Street, San Jose, California 95125, hereby declare:

1. We are joint inventors of the subject matter disclosed and claimed in United States Patent Application No. 09/942,789 filed on August 29, 2001, and titled "High Speed Network Interface With Automatic Power Management with Auto-Negotiation."

2. The embodiments of the invention disclosed in above-captioned patent application were conceived cooperatively by Nathaniel Henderson, Chi-Lie Wang, and Boadong Hu at least prior to April 24, 2001.

3. 3Com Corporation is the assignee of U.S. Patent Application Serial No. filed on August 29, 2001.

4. Accompanying this declaration is (i) Exhibit A containing a photocopy of the pages of a 3Com Invention Disclosure Form that contain a brief description of the invention and code illustrating conception of our invention; and (ii) Exhibit B containing photocopies of the pages of an estimated date for filing of the application.

5. The conception date and the revision date of the code from Exhibit A have been redacted; however, as indicated in Exhibit A, the inventors signed the declaration on February 5, 2001, which was prior to at least April 24, 2001 (i.e., the filing date of the U.S. Patent Application Pub. No. 2002/0188875.)

6. Exhibit B provides an estimated on which the application was planned to be filed. As indicated, the document in Exhibit B was faxed to 3Com Coporation on April 16, 2001, before April 24, 2001 (i.e., the filing date of the U.S. Patent Application Pub. No. 2002/0188875.)

7. As shown in Exhibit A, the inventors were employed in Santa Clara, California and we conceived and reduced to practice the invention in Santa Clara.

8. We hereby declare further that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true;

McDONNELL BOEHNEN
HULBERT & BERGHOFF LLP
300 SOUTH WACKER DRIVE
CHICAGO, ILLINOIS 60606
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and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

Date: 10/15/2007 Signed: Chi-Lie Wang
Chi-Lie Wang

Date: _____ Signed: _____
Nathaniel Henderson

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and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

Date: _____ Signed: _____
Chi-Lie Wang

Date: 10/16/2007 Signed: _____
Nathaniel Henderson

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EXHIBIT A

INVENTION DISCLOSURE FORM
3COM CONFIDENTIAL– PRIVILEGED ATTORNEY-CLIENT COMMUNICATION

IDF DOCKET NUMBER: _____

This is an Invention Disclosure Form for 3Com Corp. and all of its affiliated companies, hereafter referred to as "COMPANY."

Instructions:

- Complete all sections. Attach supplemental pages and other materials.
- Supply enough information to provide an understanding of your invention.
- Any questions regarding this form should be referred to Bill Becker (408-326-5485), Joann McCrea (408-326-2326) or Patti Contreras (847 262-3302) by phone or by e-mail (Patent IDF)
- **Return Completed Form To:** Legal Department / Patent Group - M.S 1308
  5400 Bayfront Plaza
  Santa Clara, California 95052-8145

Date Received in Legal:

***1. Title of the Invention** . . . Write a short descriptive title, avoiding coined terms and project names.

An Apparatus for Automatic Power Management for Gigabit Ethernet

***2. Inventors** Include the names of all persons who made a contribution to the conception of the invention. If there are more than five inventors, use a Supplemental Sheet.

*Formal Name:	Nathaniel Henderson	M.S. & Location	5259 cube 500.2.586
Home Address:	1329 Prevost St San Jose, CA 95125		
Home Phone:	(408) 278-9047	Work Phone:	(408) 326-7296
*Employee No.	05075	Division:	BCG
Supervisor:	Kap Soh	Department:	Core Engineering
Citizenship:	USA	:	
*Formal Name:	Chi-Lie Wang	M.S. & Location	5259
Home Address:	466 Ives Terrace, Sunnyvale, CA 94087		
Home Phone:	(408) 530-054[illegible]	Work Phone:	(408) 326-7001
*Employee No.	02659	Division:	BCG
Supervisor:	Kap Soh	Department:	Core Engineering
Citizenship:	USA	:	
*Formal Name:	Baodong Hu	M.S. & Location	5259
Home Address:	2277 Iynwood Terrace, Milpitas, CA 95053		
Home Phone:	(408) 262-6318	Work Phone:	(408) 326-5743
*Employee No.	08411	Division:	BCG
Supervisor:	Nathaniel Henderson	Department:	Core Engineering
Citizenship:	~~USA~~ china B.D.H	:	
*Formal Name:		M.S. & Location	
Home Address:			
Home Phone:		Work Phone:	
*Employee No.		Division:	
Supervisor:		Department:	
Citizenship:		:	
*Formal Name:		M.S. & Location	
Home Address:			
Home Phone:		Work Phone:	
*Employee No.		Division:	
Supervisor:		Department:	

ORIGINAL

Inventors' Initials: N.H. C.L. B.D.H _____ _____

Citizenship:

Check here and attach supplemental sheet if more than 5 inventors ☐

***3. Conception of the Invention**

Date of conception: [redacted] Location of conception: Santa Clara

Date of first written description: [redacted]

Location of such first description: Santa Clara Page(s): 1

Please attach copies of all pertinent lab notebooks or equivalent. They should be signed, dated and witnessed by two other people who have read and understood the description of the invention.

4. Reduction to Practice

Reduction to practice is merely demonstrating that an invention works, with evidence such as working models, prototypes or simulations. Reduction to practice is not necessary to file a patent application.

Date of any such reduction to practice: none planned ☐ / date/planned date of reduction to practice: [redacted]

Location of reduction to practice: Santa Clara

***5. Invention Applicability**

To which division or operation does this invention best apply?	BCG
Field of technology (e.g., manufacturing, switches, hubs, routers, network management software, adapters, etc.)	Gigabit Ethernet

***6. Related Art**

Is this invention an improvement of an existing COMPANY product? No ☒ Yes ☐

If "Yes," identify the existing product: _____

and identify the improvement _____

What was the problem to be solved?

The PCI Power Management Specification requires that network wake-up devices consume only 1.2 Watts while operational in a low-power mode. The InfiniBand specification has a similar requirement (1.3 Watts), and therefore there is a similar issue with InfiniBand. This has not been a problem for 10/100 Ethernet since these chips can be fully functional and consume less than 1.2 Watts, but gigabit Ethernet devices consume considerably more than 1.2 Watts. The problem, therefore, is how to have a gigabit Ethernet device operate as a wake-up device in compliance with the PCI Power Management Specification, and the InfiniBand Power Management Specification.

How had others attempted to solved it before you?

The present suggested solutions deal with the problem via software. I don't think anyone has attempted to solve this problem with hardware.

What were the problems or disadvantages with prior solutions?

Software solutions are only viable when software has access to the gigabit Ethernet controller. A gigabit Ethernet controller can be in operation, when software has no access to the device. In such cases only a hardware solution is viable.

What are the closest known technology, products, etc ("prior art")-list in #7 below

Ethernet PCI controllers capable of Power Management

7. Reference Materials

List any printed publications, patents, patent applications or any other materials you are aware of which provides background material and/or prior art for your invention. **Required if you know of any**

Low-Power Apparatus for Power Management Enabling (2402.IPG)

PCI Power Management Specification 1.1

InfiniBand Architeture Specification 1.0

IEEE Standard 802.3z

What other companies or inventors might have prior art

Broadcom and Alteon have had access to this invention, but have no prior art of their own.

*8. Key Words

Indicate any key words or phrases (preferably at least 3) we could use to search for related art or identify this invention for use in our own database.

Gigabit Ethernet, Power Management, Auto Negotiation, Gigabit Physical Layer, InfiniBand

*9. Drawings of the Invention

Please submit clear drawings which illustrate the invention either by electronically inserting them below or by using supplemental sheets if you cannot electronically insert them, if drawings are applicable

See attachment

*10. Brief Description of the Invention

Describe the structure, function and/or method of the invention in just enough detail to enable someone technical to understand how you solved the problem Explain how the invention solves the problem identified in Section 6 above. Stress the fundamental principle of the new idea from an engineering standpoint. You should reference any drawings you submitted to help explain the invention. If you have a detailed description, attach it electronically, if possible, (and physically on the signed copy) to the end of this IDF on the supplemental sheets.

See attachment

*11. Strategic/Tactical Value of the Invention

In a few sentences, explain how this invention will have strategic value to the company, whether in economic or non-economic terms. That is, how could such a patent help 3Com and/or how could such a patent adversely affect our competitors, both in the present and in the future?

3Com needs to strengthen its IP position in relation to its silicon/PHY vendors. Any gigabit PHY that wants to operate in a client environment will need to solve the problem that this invention solves. If we own some IP within the gigabit PHY it will give 3Com a better negotiation position with our PHY vendors.

*12. Sale/Public showing

A sale, offer for sale, public showing or release of the invention may affect COMPANY's right to patent the invention. Submit this form even if a public sale, showing or release has already occurred.

Has this invention been publicly disclosed or incorporated into a product that has been sold or offered for sale.

No ☒ Yes ☐

If "Yes," when and to whom?

If "No" is any such action anticipated and if so what is your best estimate of the date?

*13. Publication of the Invention

Publication of a description of the invention may affect COMPANY's right to patent the invention. Submit this form even if publication has occurred.

Has a description been published or is it scheduled to be published? No ☒ Yes ☐

If "Yes," when and to whom? _____

Has a description been disclosed or is it scheduled to be disclosed? No ☐ Yes ☒

If "Yes," when and to whom? **Broadcom Corporation (only orally and only a few aspects of the invention)**

Do you believe a Non-Disclosure Agreement was used? No ☐ Yes ☒

If "Yes," please attach copy if available. _____

14. Project/Release/Standards/Related disclosures Info

Project name and description:	**Medusa (Single chip Gigabit Ethernet PCI-X Controller)**
Product name and model number, if applicable:	

Does this invention relate to an actual or proposed official or defacto standard?	☐ NO ☒ YES -(name of std.) PCI Power Management 1.1, InfiniBand 1.0, and IEEE 802.3z
Please list 3Com docket numbers of all other invention disclosures that are related to this one:	**Low-Power Apparatus for Power Management Enabling (2402.IPG)**

15. Licensing/Competitive Analysis

Is this a licensable technology? No ☐ Yes ☐ Don't know ☒

If "Yes," name the fields in which this might be licensed: _____

If "Yes," name the companies which may possibly be interested: _____

16. Government Agency Contract

Was this invention made directly or indirectly under a government agency contract? No ☒ Yes ☐

If "Yes," government agency contract number: _____

***17. Joint Development or Development Contract**

Was this invention jointly developed with inventors from another company? No ☒ Yes ☐

If "Yes," please identify the company and/or non COMPANY inventors: _____

Was the invention tested, constructed or conceived pursuant to the performance of a development contract with another company? No ☐ Yes ☐

If "Yes," please identify the contract and its location: _____

16. Attorney

If there is a particular patent attorney with whom you would like to work on this disclosure, suggest his/her name. **Mark Haynes**

P.O. Box 366, Half Moon Bay , CA 94019

(650) 712-0340

***17. Signatures of Inventors**

This Invention Disclosure Form is submitted pursuant to your employee or other agreement with COMPANY. In accordance with said agreement, you have agreed to assign and hereby do assign all rights, tittle, and interest in the above described invention and any patent applications and patents based on this invention to 3Com Corporation and its subsidiaries. When completed, this form should be delivered to the 3Com Legal Department / Patent Group so that the disclosed invention can be evaluated for patentability.

The inventors listed below hereby acknowledge and agree that for purposes of administering this invention and any patent applications thereon and 3Com's interest therein, all inventor data, including, but not limited to,

Inventors' Initials: NH C-L BDH _____ _____

personal information, may be transferred to and stored in a 3Com database located in the United States to which selected 3Com employees and outside counsel in the U.S. and other countries of the world may have access

Please sign and date below and be certain that each page of this disclosure has been initialed by each inventor. Use a Supplemental Sheet if there are more than 5 inventors.

Signature: _____ Date: 2/5/2001

Signature: _____ Date: 2/5/2001

Signature: _____ Date: 2/5/2001

Signature: _____ Date: _____

Signature: _____ Date: _____

***18. Witnesses: Read and Understood**

This Invention Disclosure Form consisting of ___ pages has been read and understood by:

Name: _____ Name: _____

Signature: _____ Signature: _____

Date: _____ Date: _____

Witnesses, please initial all supplemental pages.

Attachment to Invention Disclosure Form
An Apparatus for Automatic Power Management for Gigabit Ethernet

Automatic power management for gigabit Ethernet allows wake up devices to be appropriately power managed without the intervention of software. The PCI 2.2 Bus Specification and the InfiniBand 1.0 Specification places strict power requirements on wake-up devices, but unfortunately a gigabit Ethernet adapter cannot operate at gigabit speeds and comply with these power requirements. It is possible for software to manage the power states of an adapter in order to ensure compliance, but there are many times when software becomes unavailable (OS crashes e.g. Windows, power outages, and user intervention). When software is unable to mange the power-states of an adapter, hardware must guarantee compliance in order to avoid physical damage to the adapter and the system environment.

Background

In the last few years, host adapters that communicate with any type of medium have been required to operate in a variety of power managed modes. This has become a popular trend and it only seems to be increasing in popularity (rolling blackouts notwithstanding). New standards, such as InfiniBand, have clearly dedicated much thought to the concept of power-management. The basic idea of a power-managed system consists of the following: when a host is not in use, it can be allowed to go into a lower power-state which allows for significant power savings. This is preferable to a complete shutdown, which requires a lengthy boot-up process to allow work to continue. In a low power states, a host monitors certain possible events that would cause it to 'wake-up.' These events could be a keystroke, movement of the mouse, phone ring, or a signal from a local area network (LAN). In the case of Ethernet networking, certain packets can be enabled to wake-up a host computer at any point within the network. This is a very useful feature since it allows network administrators the ability to maintain and upgrade systems from a remote location during non-working hours.

Since wake-up devices need to remain operational in order to monitor wake-up events, they are allocated power in order to perform their function. In the case of the PCI 2.2 specification this power allotment is 1.2 watts, and for InfiniBand it is 1.3 watts. In both these cases it is impossible with today's technology to maintain a gigabit Ethernet link and consume less than 1.2 watts. Cutting edge technology seems to suggest that we may see a gigabit PHY chip consuming a little less than 1.0 watt in the next few years, but a gigabit PHY is only part of the power consumption needed for a wake-up apparatus to work at gigabit speeds. Many experts would argue that we will never see a gigabit adapter consuming less than 1.2 watts. However, not being able to maintain a gigabit-link in a power-managed adapter is not an issue since a high speed networking connection is not necessary to receive a wake-up packet. When the host is

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'asleep' it is only necessary that it is able to receive a packet – how fast it gets there is of no importance, therefore gigabit adapters can negotiate to slower speeds before going to sleep.

At the present time, software manages the power states of adapters. When a host plans to go to sleep, software negotiates to slower networking speeds to save power. However, there can be times when a host attempts to be in a sleep-mode when software intervention is impossible. This can occur when the OS is inoperative or after power is restored following a power-loss. The fact that software isn't always available to manage power-states of an adapter isn't an issue with 10/100 Ethernet adapters because they can be in a fully operational state and still consume less than 1.2 watts. Since this is not the case with a gigabit Ethernet adapter a new method or apparatus is needed to power manage the adapter in the absences of software control.

It is precisely this problem that our apparatus is intended to solve.

Description of Apparatus

This apparatus was designed for a single integrated circuit implementation of a 10/100/1000 PCI Ethernet controller. We shall refer to this integrated circuit simply as the chip for this description. At the present time this apparatus has been designed and verified in HDL. The entire chip has been synthesized and laid out, but has yet to be produced in silicon form.

The most important aspects of this invention can be understood by studying the flow diagram on page 5 of this attachment. This diagram describes a state machine that always begins from the dead, or power-off, state. From any of the other states in this diagram it is assumed that a transition to the dead state can be made any time power is removed. For simplicity these state transitions were not included in the diagram.

From the *Dead State*, a transition will occur any time power is applied to the chip to enable its functionality. At this point a voltage divider circuit is used to monitor the source of the power that is being applied to the chip (POR: *Power On Reset circuit* fires). If it is observed that power is available from the PCI main power rails, the Power Management state machine will automatically transition into its *Full Power State*. In the *Full Power State* all clocks within the chip are enabled to operate at full speed and the Physical Layer or PHY (the portion on the chip dedicated to the actually transmission and reception of bits on the wire) is allowed to negotiate to the fastest speed possible. In this state the power consumed comes from the bulk source of power, not auxiliary power. Auxiliary power is limited to 1.2 watts (375ma @ 3.3V).

There are two events that can cause a transition out of the *Full Power State*. Either software places the adapter into a sleep state (D1, D2 or D3 as defined by the PCI 2.2 specification), or power is removed from the PCI main supply. If the adapter is placed into a sleep state by system software, it should have also been previously instructed to negotiate to a slower signaling speed. Since the failure of software to operate properly would lead to physical damage, it is essential that the hardware have a fail-over mechanism to save itself in the case that system software has placed it into a sleep state without renegotiating to a slower speed. (How many times does the Windows OS fail to operate properly?) In the case that the adapter has been placed into a sleep state without previously negotiating a slower operating speed, this state machine will send control signals to the PHY to force it to renegotiate to a 10/100 speed. If it is impossible to negotiate to one of these slower speeds, communication (the link) will be terminated to avoid physical damage to the adapter and/or host computer. An interesting corner case arises when the hardware automatically renegotiates to a 10/100 speed. During the negotiation process the communication link is drop momentarily, which in turn can be considered to be a 'wake-up event' by the host. This is referred to as wake on link change. If host is woken up just after it tried to put the adapter to sleep an infinite loop of sleep -> wake-up -> sleep could be entered. This situation has been avoided in our apparatus by automatically blocking the link change information to the wake-up logic in the chip during the renegotiation process. Once the PHY is running at a 10/100 speed the state machine can enter the *Low Power State*.

The other event that can cause a transition out of the *Full Power State* is the removal of the PCI Main bulk power. If this event occurs, the only power supply left is the auxiliary power. If the adapter was enabled as a wake-up device at the initial boot sequence (the PME Enable bit set in the PCI Power Management configuration register) it will be allowed to enter the *Low Power State* if it can successfully negotiate to a 10/100 speed. Otherwise the adapter must go into a *Power Down State* in which it can only consume 20ma @ 3.3V or 66mW of power. In order to achieve such extremely low power consumption, virtually the entire chip must be shut down. The PHY is completely isolated from the power source and the only clock operative in the chip is the one that goes to this state machine. All other clocks are disabled and an external signal is activated to isolate any other circuitry on the adapter board that might cause the power consumption to rise above 66Mw.

The *Low Power State* is typically entered into from the *Full Power State* as described before. However, the *Low Power State* can also be entered into from the *Dead State*, if the system is powered on using only auxiliary power. This will happen in many systems if they are in a sleep state when a power outage occurs. When power is restored, these systems will only reapply auxiliary power, they will not completely reboot. This scenario we refer to as a D3-cold power-up. If this occurs and the hardware doesn't have a self-mechanism to automatically enable itself as a wake-up device, the system will lose its capability to be

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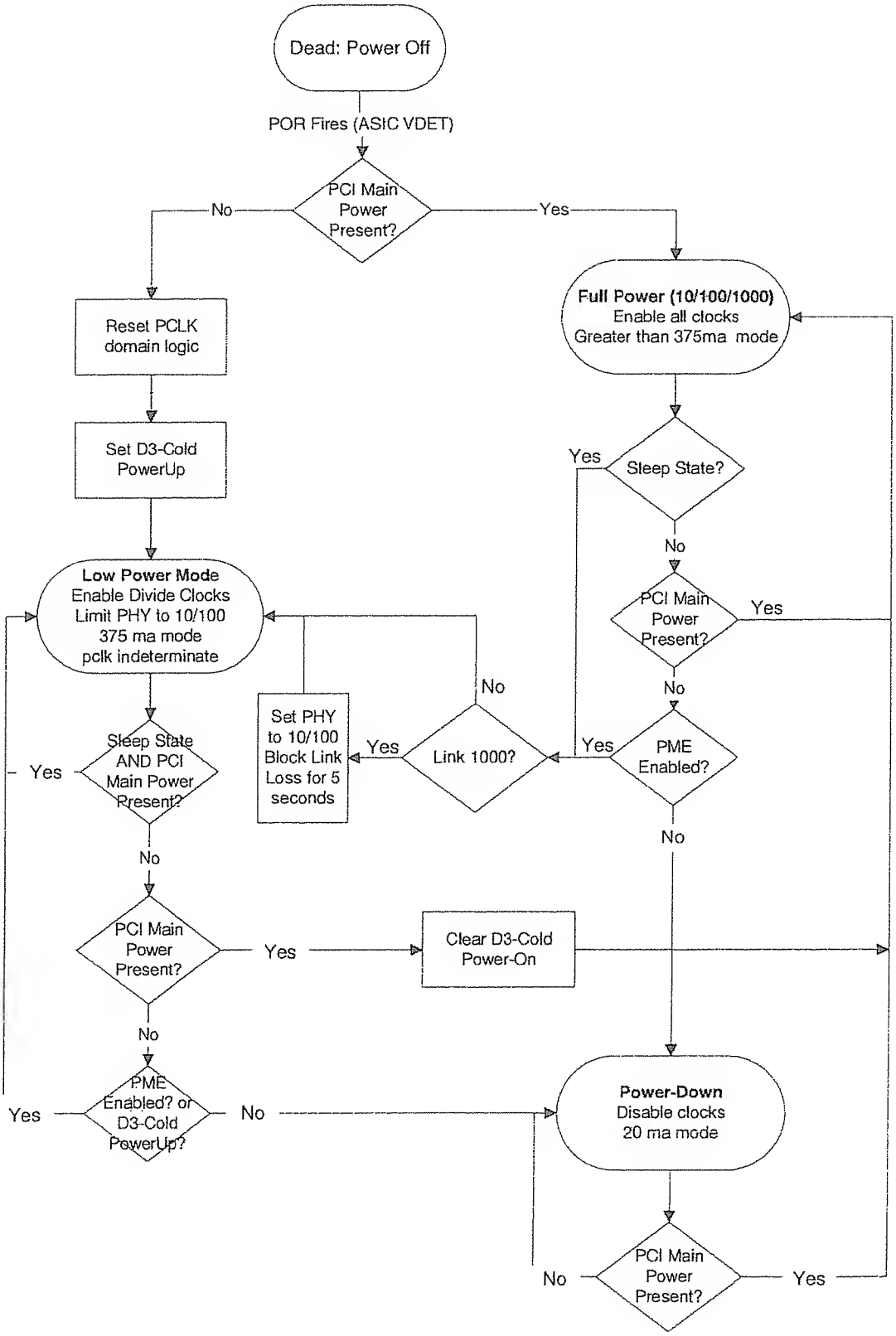
remotely managed. This could pose quite a problem for a large organization after any power outages. System vendors can ensure that there is enough auxiliary power for self-enabling of wake up functionality by ensuring that there is enough auxiliary power for every possible wake-up device, or by using an apparatus as described by 3Com IDF 2402.IPG. Given that there is enough power to perform the wake-up function, the hardware must enable itself to perform this function provided that a D3-cold power-on has occurred. The hardware enables itself during the transition from the *Dead State* to the *Low Power State* by setting the D3-cold power-on bit. This bit allows the adapter to stay in the *Low Power State* after a D3-cold power-on. The bit is cleared once main PCI power is restored, since it will no longer be needed to maintain the *Low Power State*.

It is worth noting that in order to meet the 1.2W power requirements for a gigabit adapter, the power savings don't only come from having the PHY reduce its communication speed. Almost every part of the Ethernet adapter circuitry must be modified (increased in size, speed, and power consumption) in order to delivery gigabit functionality. In order to achieve power consumption that is equivalent to a 10/100 Ethernet adapter, many other methods must be employed at the same time that the PHY portion is negotiating to a 10/100 speed (The transition from the *Full Power State* to the *Low Power State*). These methods are: 1) Turning off clocks to parts of the chip that are not in use, 2) Dividing down the clocks to a slower speed (less switching = less power consumed), and 3) Using less of the available memory.

N.A. C.L. BDH

Power Management SM



N.H. C L B.D.H

```
/*****************************************************************************/
/*                3Com Confidential and Proprietary.                         */
/*                Copyright (c) 3COM Corporation, [redacted]                 */
/*                                                                           */
/* Project:       Medusa Gigabit Ethernet ASIC                               */
/*                                                                           */
/* Module Name:   PowerManagementSM                                          */
/*                                                                           */
/* Owner:         Nathan Henderson                                           */
/*                                                                           */
/*                                                                           */
/* Description :                                                             */
/* This state-machine contains 3 states. Full-power, Low-power and           */
/* Power-down. Using the control signals from this module, the               */
/* Medusa design will meet the following power                               */
/* restrictions for the entire board: Full-power: under 1.8 amps,            */
/* Low-power: under 375ma, Power-down: under 20 ma. These current            */
/* measurements are made @ 3.3V supply to the board from the PCI bus.        */
/*                                                                           */
/*                                                                           */
/*                                                                           */
/* Revision History:                                                         */
/* Date          Name        Comments                                        */
/* --------      ----        --------                                        */
/* [redacted]    Nathan H    Initial version                                 */
/*                                                                           */
/*****************************************************************************/
module PowerManagementSM ( clk25MRaw,
                           pclk,
                           powerUpRst_clk25MRawN,
                           powerUpRst_pclkN,
                           pmPciPower_clk25MRaw,
                           hsSleep,
                           ioLink1000N,
                           pmeEn,

                           ioPowerDown_clk25MRaw,
                           ioLowPowerMode_clk25MRaw,
                           pmFullPower,
                           pmResetPci_clk25MRaw,
                           pmD3ColdPowerUp,
                           pmShortResetPhy);

input  clk25MRaw;
input  pclk;
input  powerUpRst_clk25MRawN; // This signal deasserts synchronously with clk25MRaw
input  powerUpRst_pclkN;      // This signal deasserts synchronously with pclk
input  pmPciPower_clk25MRaw;
input  hsSleep;
input  ioLink1000N;
input  pmeEn;

output ioPowerDown_clk25MRaw;
output ioLowPowerMode_clk25MRaw;
output pmFullPower;
output pmResetPci_clk25MRaw;      // One-clock pulse to start state-machine that will reset PCI domain logic
output pmD3ColdPowerUp;
output pmShortResetPhy;      // Two-clock pulse to start state-machine that will reset the PHY

parameter [2:0] // synopsys enum state_info
     DEAD       = 3'b000,
     FULLPOWER  = 3'b010,
     LOWPOWER   = 3'b101,
     POWERDOWN  = 3'b110;

reg [2:0] // synopsys enum state_info
        pmState, pmNextState;

reg       pmeEn_Q1;
reg       pmeEn_Q2;
reg       ioPowerDown_clk25MRaw;
reg       ioLowPowerMode_clk25MRaw;
reg       pmResetPci_clk25MRaw;
reg       setD3ColdPowerUp;
reg       pmD3ColdPowerUp;
reg       hsSleep_clean;
reg       pmeEn_clean;
reg       hsSleep_cleanQ1;
reg       hsSleep_clk25MRaw;
reg       pmeEn_cleanQ1;
reg       pmeEn_clk25MRaw;
reg       pmFullPower;
reg       resetPhy_clk25MRaw;
reg       resetPhy1_clk25MRaw;
reg       resetPhy2_clk25MRaw;
reg       ioLink1000N_clk25MRaw1;
reg       ioLink1000N_clk25MRaw2;
```

N.H. C.L. B.D.H

```
/* synopsys state_vector pmState

//
// The following section includes de-glitching flip-flops and synchronizers
//
always @ (posedge pclk or negedge powerUpRst_pclkN)
begin
  if (!powerUpRst_pclkN)
    begin
      pmeEn_clean   <= 1'b0;
      hsSleep_clean <= 1'b0;
    end
  else
    begin
      pmeEn_clean   <= pmeEn;
      hsSleep_clean <= hsSleep;
    end
end

always @ (posedge clk25MRaw or negedge powerUpRst_clk25MRawN)
begin
  if (!powerUpRst_clk25MRawN)
    begin
      hsSleep_cleanQ1          <= 1'b0;
      hsSleep_clk25MRaw        <= 1'b0;
      pmeEn_cleanQ1            <= 1'b0;
      pmeEn_clk25MRaw          <= 1'b0;
      ioLink1000N_clk25MRaw1   <= 1'b0;
      ioLink1000N_clk25MRaw2   <= 1'b0;
    end
  else
    begin
      hsSleep_cleanQ1          <= hsSleep_clean;
      hsSleep_clk25MRaw        <= hsSleep_cleanQ1;
      pmeEn_cleanQ1            <= pmeEn_clean;
      pmeEn_clk25MRaw          <= pmeEn_cleanQ1;
      ioLink1000N_clk25MRaw1   <= ioLink1000N;
      ioLink1000N_clk25MRaw2   <= ioLink1000N_clk25MRaw1;
    end
end


always @ ( pmState or pmPciPower_clk25MRaw or hsSleep_clk25MRaw or pmeEn_Q2 or pmD3ColdPowerUp)

begin
  pmNextState                  = pmState;
  ioPowerDown_clk25MRaw        = 1'b0;
  ioLowPowerMode_clk25MRaw     = 1'b0;
  pmResetPci_clk25MRaw         = 1'b0;
  resetPhy_clk25MRaw           = 1'b0;
  pmFullPower                  = 1'b0;
  setD3ColdPowerUp             = pmD3ColdPowerUp ;


case (pmState) //synopsys full_case

   DEAD:      begin
                if (pmPciPower_clk25MRaw)
                  pmNextState = FULLPOWER;
                else
                  begin
                    pmResetPci_clk25MRaw  = 1'b1;
                    setD3ColdPowerUp      = 1'b1;
                    pmNextState           = LOWPOWER;
                  end
              end


  LOWPOWER:   begin
                ioLowPowerMode_clk25MRaw   = 1'b1;
                if (hsSleep_clk25MRaw & pmPciPower_clk25MRaw)
                  pmNextState = LOWPOWER;
                else if (pmPciPower_clk25MRaw)
                       begin
                         pmNextState      = FULLPOWER;
                         setD3ColdPowerUp = 1'b0;
                       end
                     else if (pmeEn_clk25MRaw || pmD3ColdPowerUp)
                            pmNextState = LOWPOWER;
                          else
                            pmNextState = POWERDOWN;

              end

 POWERDOWN:  begin
               ioPowerDown_clk25MRaw      = 1'b1;
```

```
                if (pmPciPower_clk25MRaw)
                  pmNextState = FULLPOWER;
                else
                  pmNextState = POWERDOWN;
              end

  FULLPOWER: begin
                pmFullPower = 1'b1;
                if (hsSleep_clk25MRaw)
                  begin
                   pmNextState = LOWPOWER;
                   resetPhy_clk25MRaw = ~ioLink1000N_clk25MRaw2;
                  end
                else if (pmPciPower_clk25MRaw)
                       pmNextState = FULLPOWER;
                     else if (pmeEn_clk25MRaw)
                            begin
                              pmNextState  = LOWPOWER;
                              resetPhy_clk25MRaw = ~ioLink1000N_clk25MRaw2;
                            end
                          else
                            pmNextState = POWERDOWN;
              end

  endcase

end



always @ (posedge clk25MRaw or negedge powerUpRst_clk25MRawN)
begin
  if (!powerUpRst_clk25MRawN)
    pmState <= DEAD;
  else
    pmState <= pmNextState;
end

always @ (posedge clk25MRaw or negedge powerUpRst_clk25MRawN)
begin
  if (!powerUpRst_clk25MRawN)
    pmD3ColdPowerUp <= 1'b0;
  else
    pmD3ColdPowerUp <= setD3ColdPowerUp;
end


always @ (posedge clk25MRaw or negedge powerUpRst_clk25MRawN)
begin
  if (!powerUpRst_clk25MRawN)
   begin
    resetPhy1_clk25MRaw <= 1'b0;
    resetPhy2_clk25MRaw <= 1'b0;
   end
  else
   begin
    resetPhy1_clk25MRaw <= resetPhy_clk25MRaw;
    resetPhy2_clk25MRaw <= resetPhy1_clk25MRaw ;
   end
end

assign pmShortResetPhy = resetPhy1_clk25MRaw | resetPhy_clk25MRaw;

endmodule
```

N.B. CL. BOH

EXHIBIT B

3COM

Attorney Estimate Sheet

Fax to: 3Com Corporation - Legal Department, **Attn: Joann McCrea**
Fax No.: 408-326-6434

3Com Docket 3641 . BCG . US . P

Outside Counsel **Haynes & Beffel LLP**

3Com Atty: _____

OC Attorney **Haynes, Mark**

Max Filing Date _____
(unless filing must be earlier to prevent possible loss of rights)

OC Docket _____

Discl Title: AN APPARATUS FOR AUTOMATIC POWER MANAGEMENT FOR GIGABIT ETHERNET

Responsible Firm Attorney: MARK HAYNES
Attorney Fees: 8500
Patent Office Fees: 1200
Other Charges: 500
Total Application Cost Estimate: 10200
Estimated Date For Filing: 15 AUGUST 2001

Mark Haynes
Attorney

This is a not to exceed dollar amount unless otherwise approved by a 3Com attorney and is to be billed at one time after filing of the application. This amount should include all costs regarding copying and transmittals of copies of all Patent Office correspondence, documents and fees including reminders through filing.

Fax the completed estimate to 3Com legal within one week of receipt of the invention disclosure

Sample Claim (of medium scope covering the invention)

◊ Preparation and filing of the application on or before the date indicated in accordance with the above cost estimate is authorized per the undersigned; or
◊ Preparation and filing of the application is not authorized and the matter should be closed on your records

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